AMENDMENTS TO THE SPECIFICATION

Please amend Paragraph 0015, 0029, 0031 and 0033 of the Specification as set forth below:

[0015] ~~FIG. 7 is a system showing~~ FIGS. 7A and 7B show a system with one embodiment of the clock shrink circuit operating with automatic test equipment.

[0029] ~~FIG. 7 (divided over FIGS. 7A and 7B) is~~ FIGS. 7A and 7B show a schematic diagram of the pull-up stages 38 of the rise and fall mirror circuits, with such stages 38 being coupled to an automated test equipment (ATE) and control circuitry 50. However, the pull-up stage 38 and ATE and control circuitry 50 are the same as found in the prior art design of FIG. 1 and therefore will not be described in detail. The ATE is indirectly coupled to the SEL input and a gate of the first transistor 62 of each of the unitcells 60. More specifically, the ATE does not directly drive the SEL input and gates, but drives the SEL input and the gates through the control circuitry, which is known logic, to provide known control signals ctrl0, ctrl1, ctrl2, and ctrl3 (not shown). Also, ~~FIG. 7 shows~~ FIGS. 7A and 7B show the detailed schematics of the matching stage 36 and the output stage 40 shown in FIG. 4, in addition to the pull-up stage 38. In FIG. 4 the pull-up stages 38 in the rise mirror circuit 32 and the fall mirror circuit 34 are shown simplified as a single variable rise delay inverter. Based upon the control signals provided by the ATE and control circuitry 50, the pull-up stages 38 are set to introduce a phase delay into the CLOCKMID signal or the CLOCKOUT signal, depending upon which stage 38 is being considered, i.e., the one in the rise mirror circuit 32 or the one in the fall mirror circuit 34 respectively (see FIG. 4). The phase delay of each delay stage 38 is initially set in the middle range of the pull-up stages 38 and the ATE and control circuitry 50 may increase or decrease the amount of this phase delay. The more phase delay introduced, the more the output signals (CLOCKMID and CLOCKOUT) are delayed per edge respectively. In other words, the rise mirror circuit 32 only adds or subtracts delay to the rise edge of the CLOCKOUT signal (which is the fall edge of CLOCKMID signal) and the fall mirror

circuit 34 only adds or subtracts delay to the fall edge of CLOCKOUT signal. As the ATE and control circuitry 50 increases the phase delay of the pull-up stages 38, additional inverters generally are not required at the input of the NOR gate 44. In other words, once the difference in rising and falling propagation delays is corrected (compensated for) by using either 2, 4, 6, etc., inverters 46, the resulting duty cycle offset does not need to be changed with the introduction by the ATE and control circuitry 50 of differing amounts of phase shift for the CLOCKOUT signal. Note that the phase shifts of the first and second pull-up stages 38 are accumulative, but impact different edges.

[0031] Referring to ~~FIG. 7~~FIGS. 7A and 7B, the matching stage 36 includes the same components previously described with respect to FIG. 4: the non-inverting logic element 42 having at least the pair of inverters 46 and the NOR gate 44. The NOR gate 44 includes p-channel transistors P1a and P1b, which are in series and connected between the supply voltage VCC and the node 58, and n-channel transistors N1a and N1b, which are connected in parallel between the node 58 and ground. The matching stage 36 is shown with the input signal CLOCK as is the case when the matching stage 36 is used in the rise mirror circuit 32; however, when the matching stage 36 is used in the fall mirror circuit 34 the input signal is CLOCKMID. The signal on the node 58 is the CLOCKB signal, as previously shown in FIG. 4.

[0033] Referring back to ~~FIG. 7~~FIGS. 7A and 7B, the COM output of the last unitcell 60, the gate of the transistor p2, a drain of a p-channel transistor p3, a drain of an n-channel transistor n2, and an n-channel transistor n4 are commonly coupled to a node 66. The drain of the transistor p2 is connected to a node 68, the source of transistor p3 is connected to the supply voltage Vcc and a source of transistor n2 is coupled to ground. A transistor p4 has its source coupled to the supply voltage Vcc and its drain coupled to the node 68. The transistor p5 has its source coupled to the supply voltage Vcc and its drain commonly coupled with the transistor n4 and the gate of transistor p4. A transistor p6 has its source coupled to the supply voltage Vcc and its drain coupled to the node 68 and an n-channel transistor n5 in the

output stage 40. An n-channel transistor n3 has its drain connected to the node 68 and its source to ground. An inverter 70 has its input connected to a KILL signal and its output coupled to the gates of transistors n2, p6, and p3. The gates of transistors n4 and p5 are connected to a FINSEL signal. The pull-up stage 38 has input signals to control the steps and a range select as well (coarse or fine), which modulates the step sizes (for example, 60ps range for coarse versus 40ps range for fine) via the FINSEL signal. There is another feature of the pull-up stage 38 that allows the circuit to ignore an input transition so as to keep the output signal constant via the KILL signal. The most common application for the KILL signal is to remove a clock from a series, commonly known as "kill-a-clock".